VELAMMAL COLLEGE OF ENGINEERING AND TECHNOLOGY, MADURAI

Department of Information Technology

Model Exam -1

1. List the main difference between PLA and PAL.

PLA: Both AND and OR arrays are programmable and Complex, Costlier than PAL.

PAL: AND arrays are programmable OR arrays are fixed, Cheaper and Simpler.

2. List the main difference between PROM and PLA.

In some cases the number of don't care conditions is excessive, it is more economical to use a second type of LSI component called a PLA. A PLA is similar to a ROM in concept; however it does not provide full decoding of the variables and does not generates all the minterms as in the ROM.

3. List the main difference between ROM and RAM.

RAM is Random Access Memory. It is a random access read/write memory. The data can be read or written into any selected address. RAMs are called as Volatile memories because RAMs lose stored data when the power is turned OFF.

ROM is a type of memory in which data are stored permanently or semi permanently. Data can be read from a ROM, but there is no write operation. ROMs are called as Non-Volatile memories because ROMs doesn't lose stored data when the power is turned OFF.

4. What is Read and Write operation?

The Write operation stores data into a specified address into the memory and the Read operation takes data out of a specified address in the memory.

5. How many words can a12x8 memory can store?

A 12x8 memory can store 4096 words of eight bits each.

6. Define ROM and RAM.

RAM is Random Access Memory. It is a random access read/write memory. The data can be read or written into any selected address. RAMs are called as Volatile memories because RAMs lose stored data when the power is turned OFF.

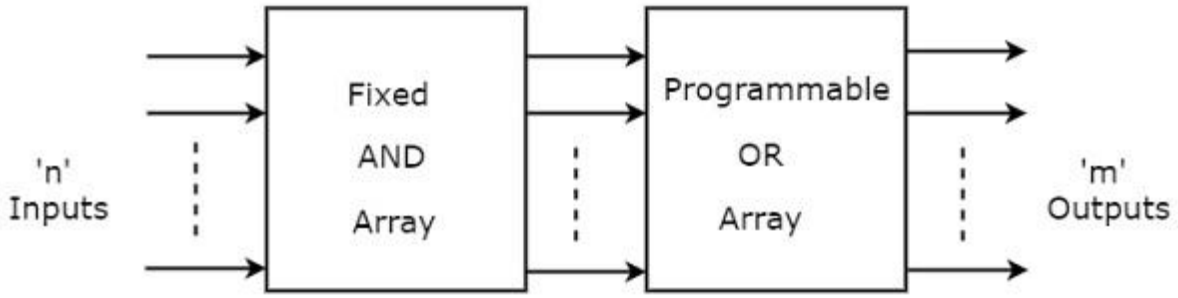
ROM is a type of memory in which data are stored permanently or semi permanently. Data can be read from a ROM, but there is no write operation. ROMs are called as Non-Volatile memories because ROMs doesn't lose stored data when the power is turned OFF.

7. Define Static RAM and Dynamic RAM.

Static RAM use flips flops as storage elements and therefore store data indefinitely as long as dc power is applied. Dynamic RAMs use capacitors as storage elements and cannot retain data very long without capacitors being recharged by a process called refreshing.

8. Define PLA.

PLA is Programmable Logic Array (PLA). The PLA is a PLD that consists of a Programmable AND array and a programmable OR array.



9. Compare Hamming code and Parity code

A parity bit is a bit appended to a data of binary bits to ensure that the total number of 1's in the data is even or odd. The simple parity code cannot correct errors, but it can detect error.

Even parity bit:

In the case of even parity, for a given set of bits, the numbers of 1's are counted. If that count is odd, the parity bit value is set to 1, making the total count of occurrences of 1's an even number. If the total number of 1's in a given set of bits is already even, the parity bit's value is 0.

Odd parity bit:

In the case of odd parity, for a given set of bits, the numbers of 1's are counted. If that count is even, the parity bit value is set to 1, making the total count of occurrences of 1's an odd number. If the total number of 1's in a given set of bits is already odd, the parity bit's value is 0.

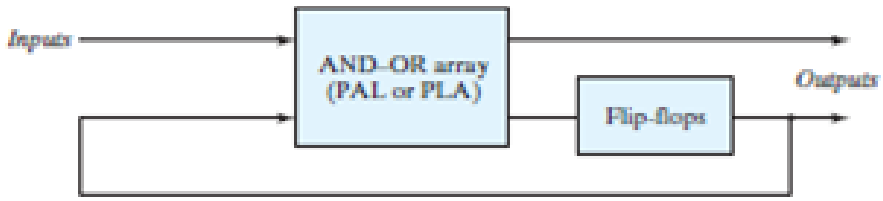
Hamming code is a set of error-correction codes that can be used to detect and correct the errors that can occur when the data is moved or stored from the sender to the receiver.

10. What is PLD?

A programmable logic device is an electronic component used to build reconfigurable digital circuits. Unlike a logic gate, which has a fixed function, a PLD has an undefined function at the time of manufacture**.**

11. Summarize about Sequential Programmable Logic Device.

The SPLD includes flip-flops, in addition to the AND–OR array, within the integrated circuit chip. The result is a sequential circuit as shown in Fig. A PAL or PLA is modified by including a number of flip-flops connected to form a register. The circuit outputs can be taken from the OR gates or from the outputs of the flip-flops.



12. Summarize about FPGA.

- A field-programmable gate array (FPGA) is a VLSI circuit that can be programmed at the user's location.
- A typical FPGA consists of an array of millions of logic blocks, surrounded by programmable input and output blocks and connected together via programmable interconnections.
- A typical FPGA logic block consists of lookup tables, multiplexers, gates, and flip-flops. A lookup table is a truth table stored in an SRAM and provides the combinational circuit functions for the logic block.

13. Define Asynchronous sequential circuit.

In asynchronous sequential circuits change in input signals can affect memory element at any instant of time.

The circuit is considered to be asynchronous if it does not employ a periodic clock signal to synchronize its internal changes of state. Therefore the state changes occur in direct response to signal changes on primary (data) input lines, and different memory elements can change state at different times.

14. Compare synchronous & Asynchronous sequential circuits.

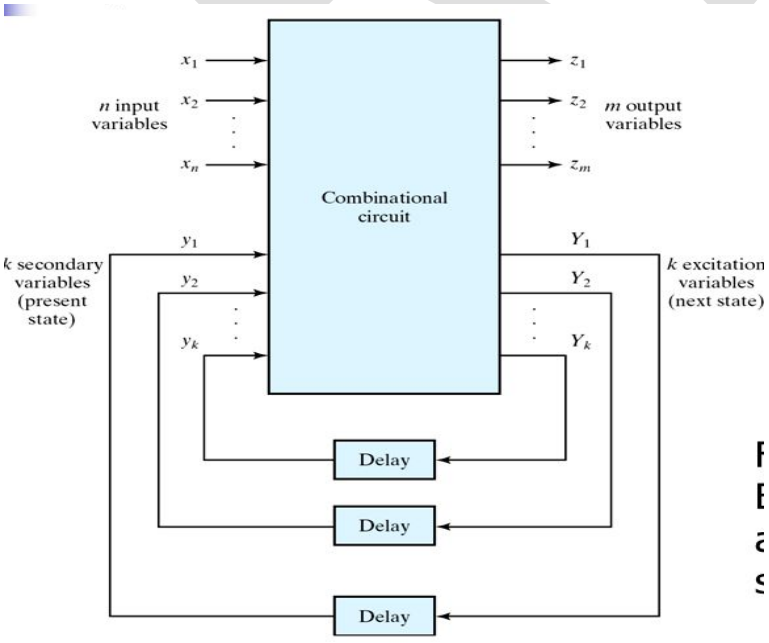
Synchronous Sequential Circuit	Asynchronous Sequential Circuit
It is easy to design.	It is difficult to design.
A clocked flip flop acts as memory element.	An unclocked flip flop or time delay is used as memory element.
They are slower as clock is involved.	They are comparatively faster as no clock is used here.
The states of memory element are affected only at active edge of clock, if input is changed.	The states of memory element will change any time as soon as input is changed.

15. Summarize about one hot state assignment.

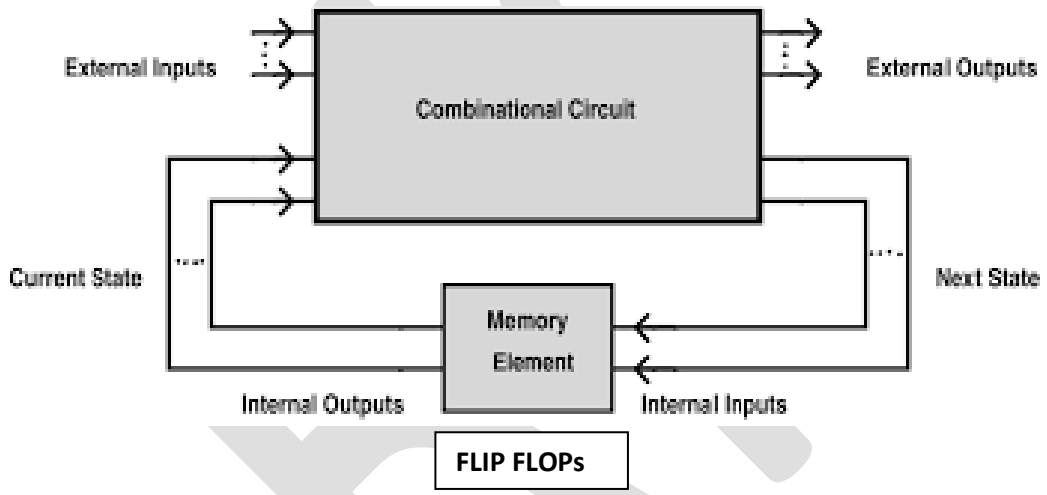
The one hot state assignment is a method for finding a race free state assignment. In this method, only one variable is active or hot for each row in the original flow table, i.e., it requires one state variable for each row of the flow table. Additional row are introduced to provide single variable changes between internal state transitions.

16. What is fundamental mode sequential circuit?

- Fundamental mode - only one input can change at a time.
- Inputs are levels and not pulses
- Dealy lines are used as memory elements



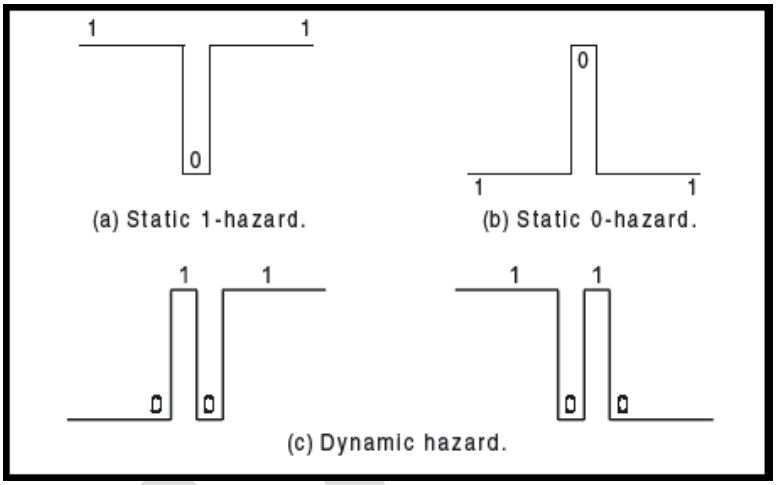
17. What is pulse mode sequential circuit?



- The input variables are pulses instead of levels.
- The pulses should not occur simultaneously on two or more input lines.
- Flip Flop are commonly used as a memory element.
- Input variables are used only in the uncomplemented or complemented forms, but not both.

18. What is Hazard and explain its types?

Hazard is an unwanted switching transient.



Some combination of propagation delays, output of that digital circuit may momentarily go to 0 when it should remain a constant 1. Then we can say the network has a static 1-hazard.

Similarly, if any digital circuit give output may momentarily go to 1 when it should remain a constant 0, then we say that the digital circuit has a static 0-hazard. Static 0- and 1-hazards can be eliminated by adding additional gates to the network to produce the missing 1-terms and 0-terms. (Additional minters).

If any digital circuit, the output is supposed to change from 1 to 0 (or 0 to 1), the output may change three or more times, we say that the digital circuit has a dynamic hazard.

19. What are the steps for the design of asynchronous sequential circuit?

- Construction of a primitive flow table from the problem statement.
- Primitive flow table is reduced by eliminating redundant states using the state reduction
- State assignment is made
- The primitive flow table is realized using appropriate logic elements.

20. What are races?

When 2 or more binary state variables change their value in response to a change in an input variable, race condition occurs in an asynchronous sequential circuit

21. Define flow table in asynchronous sequential circuit.

In asynchronous sequential circuit state table is known as flow table because of the behavior of the asynchronous sequential circuit. The stage changes occur in independent of a clock, based on the logic propagation delay, and cause the states to flow from one to another.

22. Define merger graph.

The merger graph is defined as follows. It contains the same number of vertices as the state table contains states. A line drawn between the two state vertices indicates each compatible state pair. It two states are incompatible no connecting line is drawn.

23. When do race conditions occur?

Two or more binary state variables change their value in response to the change in input variable.

24. What is the significance of state assignment?

In synchronous circuits-state assignments are made with the objective of circuit reduction. Asynchronous circuits-its objective is to avoid critical races.

25. What is shift register?

In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the 'data' input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the 'bit array' stored in it.

26. Show the block diagram of PISO shift register.

In Parallel In Serial Out (PISO) shift registers, the data is loaded onto the register in parallel format while it is retrieved from it serially.

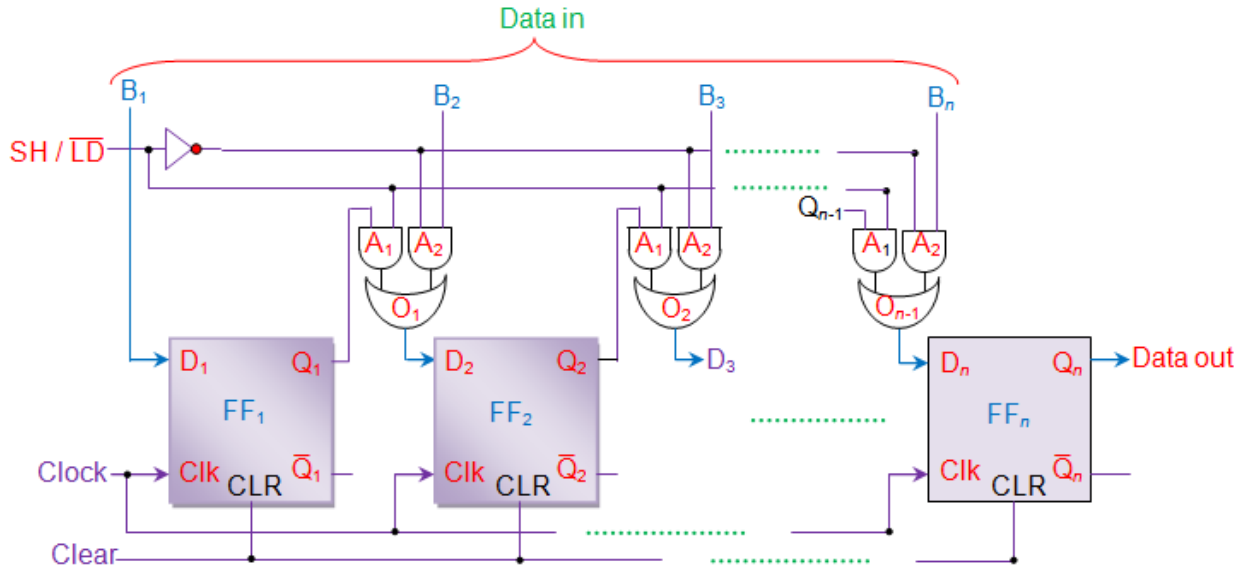
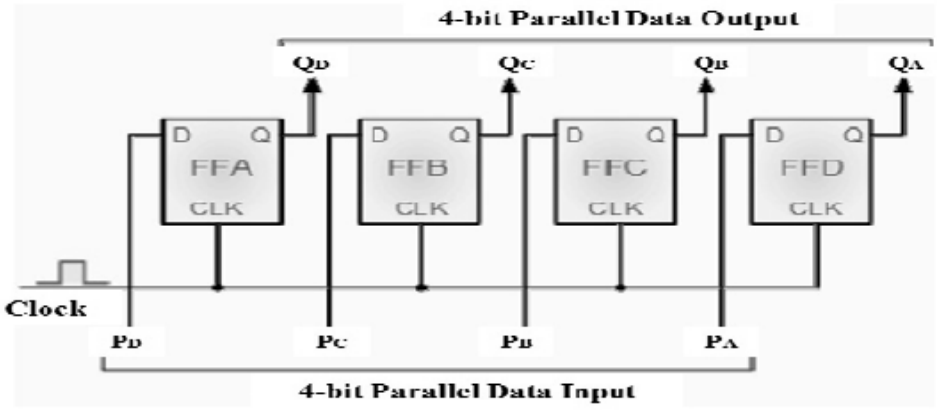


Figure 1 *n*-bit Parallel-In Serial-Out Right-Shift Shift Register

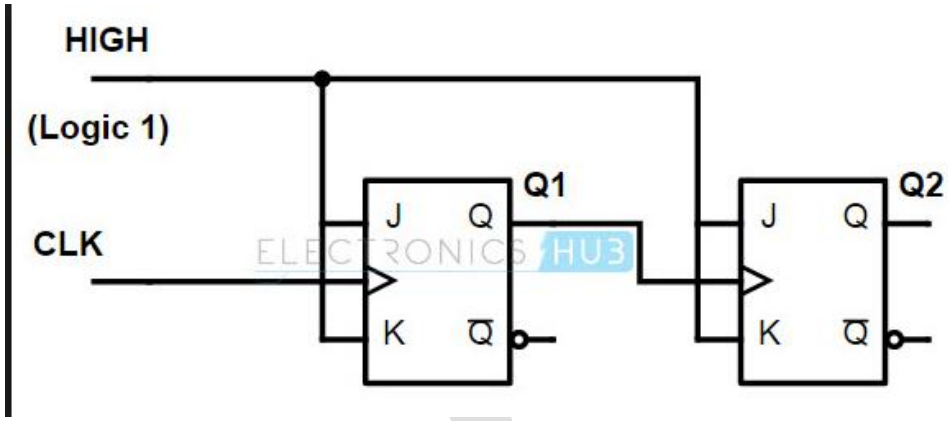
Here $SH/\overline{LD}$ control line is used to select the functionality of the shift register amongst shift or load at a given instant of time.

27. Show the block diagram of PIPO shift register.

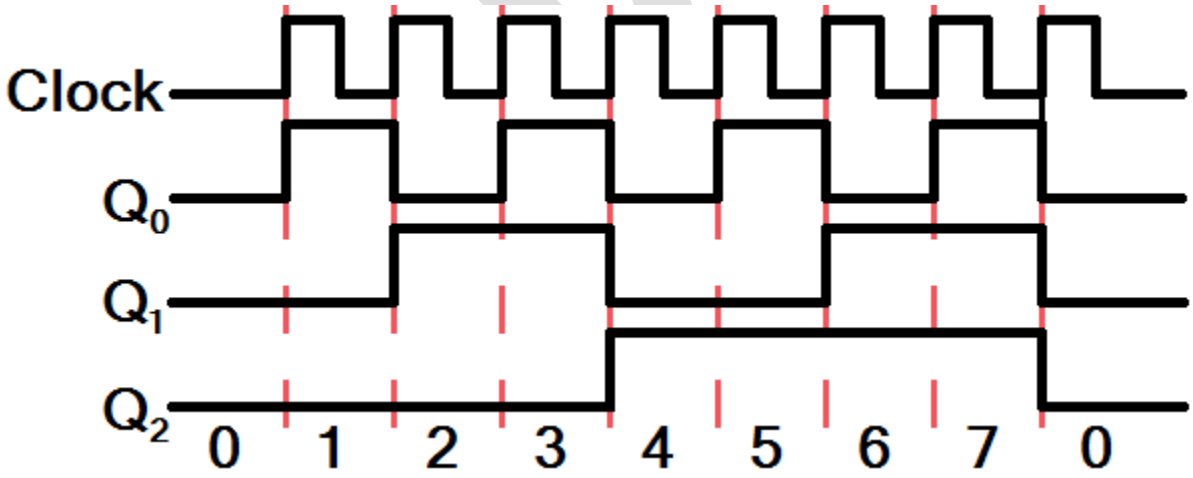


The parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

28. Show the block diagram of 2 bit synchronous counter.



29. Show the timing diagram of 3 bit synchronous counter.



30. Show Mod -2 counter using D flip flop.

PART B

11. Build the following multi-Boolean function using PLA PLD.

- Definition of PLA - 1 Marks
- K MAP Simplification – with reason – 4 Marks
- PLA Implementation table – 4 Marks
- Circuit Diagram -4 Marks

Build 3 bit Binary to Gray code converter and implement using PLA.

- Definition of PLA - 1 Marks
- Conversion table - 3 Marks
- K MAP Simplification – 3 Marks
- PLA Implementation table – 3 Marks
- Circuit Diagram -3 Marks

Implement the switching function using a 5 x 8 x 4 PLA

- Definition of PLA - 1 Marks
- K MAP Simplification – with reason – 4 Marks
- PLA Implementation table – 4 Marks
- Circuit Diagram -4 Marks

12. Build the following Boolean function using PAL.

- Definition of PAL – 1 Mark
- K MAP Simplification – 5 Marks
- PAL Program table – 5 Marks
- Circuit Diagram - 2 Marks

Construct an Even parity bit generator and checker with an example.

- Definition for parity bit, odd and even parity bit – 3 marks
- Even Parity Generator – 3 Marks
- Even Parity Generator – K Map and Circuit – 2 Marks
- Even Parity Checker – 3 Marks
- Even Parity Checker – K Map and Circuit – 2 Marks

13. Construct an odd parity bit generator and checker with an example.

- Definition for parity bit, odd and even parity bit – 3 marks
- Odd Parity Generator – 3 Marks
- Odd Parity Generator – K Map and Circuit – 2 Marks
- Odd Parity Checker – 3 Marks
- Odd Parity Checker – K Map and Circuit – 2 Marks

Hamming code

- Definition – 2 Marks

- Construction of bit location table – 5 Marks
- Check for parity bits – 5 Marks
- Corrected code - 1 mark

14. Hazards in Combinational / Sequential circuit (7) Marks

(1)

- Definition for Hazards – 1 Mark
- Circuit diagram with variables and equation – 1 Mark
- Case 1 and Case 2—Values and Explanation for case1 and case2 – 1 Mark
- Timing diagram – 1 Mark
- Types of hazards with diagram - 1 Mark
- Elimination of hazards: Definition And K- MAPs - 1 Mark
- Circuit Diagram – Hazard free circuit – 1 Mark

(2) Problem in Hazards

K Map for Hazard Circuit – 2 Marks

K Map for Hazard Free Circuit – 2 Marks

Circuit for Hazard Free Equation – 1 Mark

15. Asynchronous sequential circuit.

- Definition of Asynchronous circuit – 1 Mark
- Circuit – 3 Marks
- State Table - 5 Marks
- Transition Table – 2 Marks
- Output Map – 2 Mark

Design of Asynchronous sequential circuit

- Definition of Asynchronous circuit – 1 Mark
- State Diagram – 5 Marks
- Primitive Flow table - 2
- Merger Graph - 2
- Reduced flow table -2
- Transition Table - 1

PART C

1. 3 bit synchronous up/Down counter.

- Definition for counter – 1 Mark
- Truth Table – 6 Marks
- K Map for Flip flop output – 6 Marks
- Circuit diagram – 2 Marks

2. Build SISO, SIPO circuit and explain in detail with an example.

- **Definition for shift register – 2 Mark**
- **Construction – 5 Marks**
- **Explanation with an example – 6 Marks**
- **Clock pulse – 2 Marks**

3. Construct 3 bit synchronous counter.

- Definition for counter – 1 Mark
- Construction using JK – 6 Marks
- Explanation – 6 Marks
- Timing Diagram - 2